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Within Your Design

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Application on Altera

StratixIV GX

Introduction to the

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~~Cost FPGA Fun and~~

~~Easy Ethernet - How~~

~~the Ethernet Protocol~~

~~Works See PCI~~

~~Express Hard IP~~

~~Demo on Low-Cost~~

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~~acceleration using~~

~~Intel Stratix 10 FPGAs~~

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2018, Dallas, Texas

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on an FPGA? FPGA*

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LEDs on DE1 Altera  
Board 5 Easy Steps  
to Building an  
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System Inside an  
FPGA Design a Block  
RAM Memory in IP  
Integrator in Vivado  
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**core evaluation on  
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Reuse with the Intel®  
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Software

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IP Core Device ...

Altera AES IP Core -

Design And Reuse

The core can be

mapped to any Intel®

FPGA Family and

optimized to suit the

particular project's

requirements. The

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synthesizes to 1,180  
ALMs. On

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mapping tables and  
QAM/PSK  
constellations.  
SHA-256 Fast IP

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Core for ASIC and

FPGA - Mercora

Technologies IP

Cores has announced

shipments of an

FPGA version of the

MACsec statistics add-

on core for its popular

MSP10 MACsec

encryption/decryption

core for line-speed

MACsec processing

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and ALTLVDS\_RX IP

Cores. LVDS

SERDES Intel FPGA

IP User Guide

Archives

**LVDS SERDES Intel  
FPGA IP User Guide**

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Altera offering to Altera FPGA users”, says Jean-Francois Nivart, CSO of intoPIX. “Our Altera IP-cores will address the increasing customer demand for our high performance JPEG 2000 real-time encoder and decoder cores and directly benefit from the access to the fast



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growing Altera market share.”

**intoPIX - PR**

**-JPEG2000 IP cores**

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**Devices**

Intel FPGA and its Intellectual Property partners offer a large selection of off-the-shelf IP cores and reference designs optimized for Intel

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Security IP cores for  
variety of AES modes,  
including AES-based  
ECB/CBC/OCB/CFB,  
AES-GCM and AES-

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XTS cores, flow-through AES/CCM cores with header parsing for IEEE 802.11 (WiFi), 802.16e (WiMAX), 802.15.3 (MBOA), 802.15.4 (Zigbee), public-key accelerators for RSA and elliptic curve cryptography (ECC ...

**IP Cores, Inc:**

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**Security, FEC,  
Compression, and  
DSP IP ...**

The AES-P IP core implements the FIPS-197 Advanced Encryption Standard. It can be programmed to encrypt or decrypt 128-bit blocks of data, using 128-, 192-, or 256-bit cipher-key. The Block Cipher mode of operation is

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run-time

programmable to  
ECB, CBC, CFB,  
OFB, or CTR.

**Programmable  
Block Cipher Mode  
AES IP Core**

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## **Floating-Point IP Cores User Guide**

The SHA256 IP core is a high performance implementation of the SHA-256 Message Digest algorithm, a one-way hash



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function, compliant with FIPS 180-2. The core is composed of two main units, the SHA256 Engine and the Padding Unit as shown in the block diagram. The SHA256 Engine applies the SHA256 loops on a single 512-bit message block, while the Padding Unit splits the input

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message into 512-bit blocks and performs the message padding on the last block of the message.

### **SHA-256 IP Core Secure Hash Function - Alma Technologies**

Altera AES IP Cores perform data encryption and/or decryption as

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specified by the Federal Information Processing Standard (FIPS) 197, Advanced Encryption Standard (AES).

### **Altera AES IP Core - Design And Reuse**

The Embedded IP Suite is a value bundle of Intel's most popular embedded IP cores and software.

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Altera Embedded IP Suite contains all the building blocks for your embedded design, including the Nios II processor, DDR/DDR2/DDR3 memory controllers, a 16550 compatible UART, and a complete Ethernet solution with the Intel® FPGA IP for Triple-Speed ...

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## **Nios® II Processors for FPGAs - Intel® FPGA**

The AES core implements Rijndael cipher encoding and decoding in compliance with the NIST Advanced Encryption Standard. It processes 128-bit data blocks with 128-bit key (a 256-bit

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key version is available). Basic core is designed only for encryption and is the smallest available on the market (less than 3,000 gates).

## **AES IP Core: Ultra-Compact Advanced Encryption Standard**

...

2.1. Installing and Licensing Intel FPGA

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### Fpga Ip Cores

IP Cores. The Intel Quartus Prime software installation includes the Intel FPGA IP library. This library provides many useful IP cores for your production use without the need for an additional license. Some Intel FPGA IP cores require purchase of a separate license for

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Processing with Field  
Programmable Gate  
Arrays Embedded  
Microprocessor  
System Design using  
FPGAs Processor  
Design  
Reconfigurable  
Computing:



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